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Overview of Semiconductor Fabrication Technology

Basic Processes:

Wafer Growth Creation of single-crystal substrate material

Photolithography Definition of regions (through a mask) on wafer for selective processing

Doping Addition of desired impurities near the surface of the wafer

Oxidation Thermal growth of natural dielectric layer (e.g. Si O_2)

Deposition Addition of layers of a specific material (e.g. Si N) on the wafer surface

Etching Removal of material from the wafer surface

Epitaxial Growth Reordering of deposited material to form single-crystal material

Wafer Growth:

Semiconductor devices and circuits are formed in thin slices of a material (called a *wafer*) that servers as the *substrate*. For proper operation of the device/circuit, the material must be formed from a single material with the crystals formed by the atoms all aligned in a specific direction. Such a material is defined as a *single-crystal* substrate. The proper alignment of the crystal lattice has a large effect on the material properties of the substrate including its electrical properties and how it reacts to other materials and chemical processing.

- Create large ingots of semiconductor material by heating, twisting, and pulling.

(~ 1-2 meters long by 10-20 cm diameter)

- Entire ingot aligned to the same crystal lattice orientation (single-crystal).
- Remove all impurities → all one element.
- Slice ingot into very thin (~400-750μ m) discs called wafers.
- Some wafer are uniformly doped with specific impurities

(e.g. Boron for p-type wafer with $N_A = 10^{14}$ cm^{-3})

Photolithography

Many steps in the semiconductor fabrication process should only affect specific areas of the wafer. To define the desired areas on the wafer (and block the remaining areas) a series of *masking layers* are used. The process of photolithography involves the use of a material called *photoresist* (PR) to generate a specific pattern on the surface of the wafer. Photoresist is a light-sensitive material which can be processed into a specific pattern after being exposed to light energy in the shape of the desired pattern. (The process is somewhat similar to photography where light energy forms a pattern on the film.) Once the PR has been patterned, the wafer will be covered by PR only in specific areas while the remainder of the wafer is uncovered. Subsequent process steps will affect only the uncovered areas where there is no PR. The process allows us to transfer shapes that are created using CAD software onto the surface of the wafer with submicron resolution. Photolithography is useful because it can transfer the pattern to the wafer surface very quickly. Direct-write methods (similar to those used to create the optical mask) produce the same results but can take several hours move across the entire surface of the wafer.

- Transfer desired pattern to an *optical mask* that is clear except where a pattern/shape is desired.
- Cover the entire wafer surface with photoresist (~1μ m thick).
- Expose the wafer to light through the optical mask (takes ~ 1-5 seconds exposure).
- Use chemical processing to remove PR only where it has been exposed to light.

(the pattern is now transferred from the optical mask to the wafer surface)

- Subsequent process steps (e.g. oxidation, diffusion, deposition, etching) will affect only the areas where there is no PR and be blocked where the PR remains.
- After all necessary processing through pattern, remove all PR in chemical process.

Doping

The operation of semiconductor devices requires that specific regions of the substrate be doped n-type of p-type with specific dopant concentrations. There are two primary methods used to add impurities (i.e. dope) the substrate: diffusion, and implantation.

Diffusion

A masking layer (e.g. PR) is used to block the wafer surface except where the dopants are desired. The wafer is placed in a *high-temperature* furnace (~1000° C) where the atmosphere contains the desired impurity in gaseous form. Through the process of diffusion, impurity atoms, which are in high concentration in the atmosphere, will diffuse into the substrate, where they have a low concentration (initially zero). After some time (~0.5 – 10 hours) the impurity atoms are uniformly distributed into the exposed wafer surface at a shallow depth (0.5 - 5μ m) at a concentration that can be reliably controlled (~10^{12}-10^{19} cm^{-3}).

Implantation

Implantation is functionally similar to diffusion, but here the atoms are "shot" into the wafer at high velocity (across a very strong electric field) and they embed themselves into the wafer surface. A short (~10min.) *annealing* step at elevated temperatures (~800° C) is used to fit the new atoms into the substrate crystal lattice. Implantation is more uniform across the wafer than diffusion and allows for very precise control of where the impurities will be. In addition, its peak concentration can be beneath the wafer surface, and it does not required a long period of time at high temperature (which can be harmful). However, an implanted junction must remain near the surface of the wafer (~ 0.1 - 2μ m) and cannot go as deep as a diffused junction. The impurity concentration profile (concentration vs. depth) is different for diffusion and implantation, however both are well known and predictable.

Resistance of a doped region

The concentration of impurities in a semiconductor determines a property called *resistivity*, ρ , which is given by

$\rho = 1 / (q \mu_n N_D)$ n-type region

$\rho = 1 / (q \mu_p N_A)$ p-type region

The electrical *resistance* of a region which has been doped by impurities is given by

$$R = (\rho L) / (W t)$$

where t is the thickness of the doped region, W the thickness, and L the length.

Oxidation

Insulating dielectric layers are a key element in semiconductor fabrication which provide isolation between conductive layers on the surface of the wafer. In fact, one of the most important reasons Silicon has become such a successful medium for integrated microelectronics is that has a good *native oxide*, which means that Silicon oxidizes (combines with elemental Oxygen) to from a dielectric oxide called silicon dioxide, SiO_2. SiO_2 is a good insulating layer and can be created by exposing Si to an O_2 environment. At elevated temperatures (~1000° C) the oxide grows quickly, which is another characteristic that makes it useful in semiconductor fabrication. Native oxides grown at elevated temperatures are referred to as *thermal oxides*. An advantage of native thermal oxides such as SiO_2 is that they have similar material properties (e.g. thermal expansion coefficient, lattice size, etc.) of the native material. This means that oxides can be grown without creating significant stresses in the material which could lead to serious problems including circuit failure. Thermal oxide grown in Si can be masked by PR, although better results can be obtained if SiN is used to mask thermal oxidation.

- When a Si wafer is exposed to O_2 at high temperatures (~1000° C) a native oxide is grown on the surface of the wafer.
- Because material (O_2) is being added to the wafer, the wafer grows in thickness, and ~ 50% of the oxide grows beneath the surface and the other half on top of the (original) surface.
- Native oxide growth is used in MOS fabrication to grow the field oxide (the region outside of the active region) and to create the gate oxide layer, the thickness of which can be well controlled.

Deposition

The addition of material to the top of the wafer to from, for example, interconnects between devices and insulators between interconnect layers, require process step generally referred to as *deposition*. A variety of material can be deposited including conductors, insulators, and semiconductor materials. Several different techniques are employed for deposition, but the process can generally be thought of as a uniform sprinkling of material on the surface of the wafer, either over the entire surface or through a masking layer (for deposition on selective areas). Two common techniques are *Chemical Vapor Deposition (CVD)* which chemically vaporizes the material to be deposited, and *Low Pressure CVD (LPCVD)* which is a similar process done near vacuum. The vaporized material then floats down to the wafer surface where it solidifies to form the deposited layer.

Dielectric Deposition

Native oxides are only available when native material is still on the surface. Thus, once a wafer has been covered with other materials (e.g. metal), a native oxide can no longer be grown. In addition, after some materials (e.g. metal) have been deposited on the wafer, the wafer can no longer be subjected to high temperatures, which are required to grow native oxides but can melt other materials used in semiconductor fabrication. Thermal oxides are also limited to thin layers (< 1 μ m). For these three reasons, it is necessary to use deposited dielectrics to cover the wafer and form insulation layers. Deposited dielectrics offer a wide variety of insulating materials including SiO_2 and SiN, they can be deposited on top of any material including metal, and they can be deposited in thick layers (~1-2 μ m) to reduce the capacitance between interconnect layers.

- Offer a variety of dielectric materials including SiO_2 and SiN.
- Can be deposited on top of all other materials used in semiconductor fabrication.
- Can be deposited in thick layers (~1-2 μ m).

Polysilicon

Polysilicon is a Silicon material that is granular and is not single-crystal like the substrate wafer. It is generally doped to act as a conductor and is used as an interconnect layer and as the gate terminal of an MOS transistor. Although metal is a better conductor (lower resistance), the primary advantages of polysilicon over other conductors are that it can withstand subsequent high temperature steps, a native oxide can be grown on top of polysilicon, and it has similar material properties to Si and SiO_2. In addition, it can be doped to set the resistance of the polysilicon layer so that is can act as a conductor or as a high-resistance layer used to from integrated resistors. Modern MOS processes typically have two polysilicon layers, one for transistor gates and short interconnects separated by a thermal oxide to the second layer used for resistors, capacitors, and memory cells like EPROM and EEPROM.

- Granular Si with similar material properties to single-crystal Si and SiO_2.
- Native thermal oxide, SiO_2 , can be grown on top of polysilicon.
- Can withstand subsequent high temperature steps (unlike metal)
- Can be doped to set resistance (low for interconnects, high for resistors)
- Used to form MOS gates, resistors, capacitors, and memory cells.

Metals

Various types of elemental metal (e.g. aluminum, gold, copper, nickel, titanium), metal alloys, and other metal compounds are used to from interconnection layers in semiconductor fabrication. A modern process typically has 2-3 metal layers (and can have as many as 7!) serving as low resistance connections between semiconductor devices or carrying current from one circuit block to the next across the circuit die. Metals are generally deposited through evaporation or sputtering to cover the entire wafer before being patterned to from all interconnects in one process step (one step per metal layer). Although most metals have a low melting temperature and must therefore be deposited after all high temperature steps (e.g. diffusion, oxidation), they are very conductive and provide low resistance interconnections even in very thin layers ($< 1\mu$ m). Depositing metal interconnect layers are typically the last steps preformed in the semiconductor fabrication process. The individual layers are insulated from each other by deposited dielectric layers with vertical openings (contacts) called *vias* that connect layers at the required points.

- Form low resistance interconnections.
- Can not withstand high temperature process steps.
- Many metal interconnect layers can be used which are insulated by deposited dielectrics.

Etching

Etching refers to the removal of material from the surface of a wafer using a chemical or mechanical process, or a combination of both. Etching processes are needed to pattern deposited layers (e.g. etch metals leaving behind only the desired traces) and form contact opening in dielectric layers (e.g. to connect a metal layer to the substrate through the dielectric). Chemical etching processes will attack (etch) some materials more quickly than others while mechanical etching will etch all material equally. Both processes require a masking layer (generally either PR or oxide) to block regions where etching is not desired.

Chemical Etching

Most materials, including Si, SiO2, PR, Polysilicon, and Metal, can be selectively removed by chemical processes that attack only the desired material. This allows the etching process to stop once the desired material has been removed (rather than continuing all the way through the wafer!). Chemical etchants can typically be blocked by masking layers of PR or oxide of appropriate thickness. The primary disadvantage of chemical etching is that it is *isotropic* (i.e. it etches in all directions -not

just vertically) and will undercut the masking layer which is undesirable in many cases.

- Selective etching of desired material.
- Can be masked by PR or oxide.
- Isotropic etch will undercut masking layer.

Chemical-Mechanical Etching

Reactive ion etching (RIE) is the primary technique of chemical-mechanical etching in which ions in a plasma bombard the surface and etch away material. The plasma can be chosen to selectively etch one material more than another. RIE is a very common process in modern semiconductor fabrication and is typically used for contact openings through dielectrics.

- Mechanical etching process with some chemical selectivity.
- Can be masked by PR or oxide.
- Anisotropic etch → no undercut.

Mechanical Etching

Purely mechanical etching processes such as *Ion Milling*, are not material selective; they bombard the wafer surface and remove any material they strike. However, a thick high-strength mask material can be used to block the etching process from the surface so that only specific areas on the wafer are etched. Because there is no chemical undercutting, mechanical etching creates a straight vertical etching profile.

- No material selectivity, must be blocked by thick mask.
- Anisotropic etch → no undercut.

Epitaxial Growth

Epitaxial growth describes the process of creating single-crystal Silicon from a thick layer of deposited Silicon (polysilicon). When the deposited Silicon is uniformly doped, the resulting single-crystal epitaxial layer will have a constant doping profile (unlike that created by diffusion or implantation) which is necessary for the formation of some semiconductor devices. An "epi" layer can be formed after initial diffusion processes to leave a "buried layer" often used in making Bipolar transistors (BJTs). The process for creating a single-crystal epitaxial layer from the deposited material is somewhat complex and involves the use of a "seed crystal" that allows an annealing process to align the crystals of the deposited material.

- Create single-crystal material from deposited (non-single-crystal) material
- Epitaxial layer has constant doping profile.
- Epi doping can be higher or lower than substrate doping, and of same of opposite type as substrate.
- Epi layer can be very thick (~1-20 μ m).
- Epi layer formed by annealing a deposited layer from a "seed crystal"

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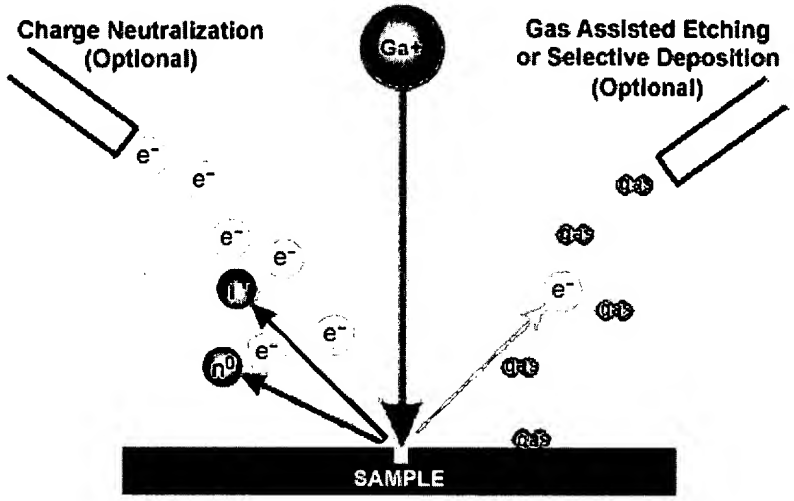
Introduction: Focused Ion Beam Systems

Focused ion beam (FIB) systems have been produced commercially for approximately ten years, primarily for large semiconductor manufacturers. FIB systems operate in a similar fashion to a scanning electron microscope (SEM) except, rather than a beam of electrons and as the name implies, FIB systems use a finely focused beam of gallium ions that can be operated at low beam currents for imaging or high beam currents for site specific sputtering or milling.

As the diagram on the right shows, the gallium (Ga^+) primary ion beam hits the sample surface and sputters a small amount of material, which leaves the surface as either secondary ions (i^+ or i^-) or neutral atoms (n^0). The primary beam also produces secondary electrons (e^-). As the primary beam rasters on the sample surface, the signal from the sputtered ions or secondary electrons is collected to form an image.



At low primary beam currents, very little material is sputtered; modern FIB systems, such as our Micrion systems, can achieve 5 nm imaging resolution. At higher primary currents, a great deal of material can be removed by sputtering, allowing precision milling of the specimen down to a sub micron scale.

If the sample is non-conductive, a low energy electron flood gun can be used to provide charge neutralization. In this manner, by imaging with positive secondary ions using the positive primary ion beam, even highly insulating samples may be imaged and milled without a conducting surface coating, as would be required in a SEM.

In addition to primary ion beam sputtering, our system permits local "flooding" of the specimen with a variety of gases. These gases can either interact with the primary gallium beam to provide selective gas assisted chemical etching or selective deposition of either conductive or insulating material by decomposition of the deposition gas by the primary ion beam.

Until recently, the overwhelming usage of FIB has been in the semiconductor industry. Such applications as defect analysis, circuit modification, mask repair and transmission electron microscope sample preparation of site specific locations on integrated circuits have become commonplace procedures. The latest FIB systems, such as our Micrion systems, have high resolution imaging capability; this capability coupled with in situ sectioning has eliminated the need, in many cases, to examine FIB sectioned specimens in the SEM.

As well as offering a full suite of semiconductor FIB services such as device modification, probe pad formation and TEM specimen preparation, Fibics Incorporated has pioneered a number of applications of FIB in materials science. These applications extend from site specific TEM specimen preparation of "difficult" materials, such as thin coatings of TiN on high speed steel through to applications in measurement of crack growth and aspect ratio during stress corrosion cracking, deformation of metal matrix composites, adhesion of polymer coatings, et cetera.

If you have any further questions about Focused Ion Beam Systems, please contact us.

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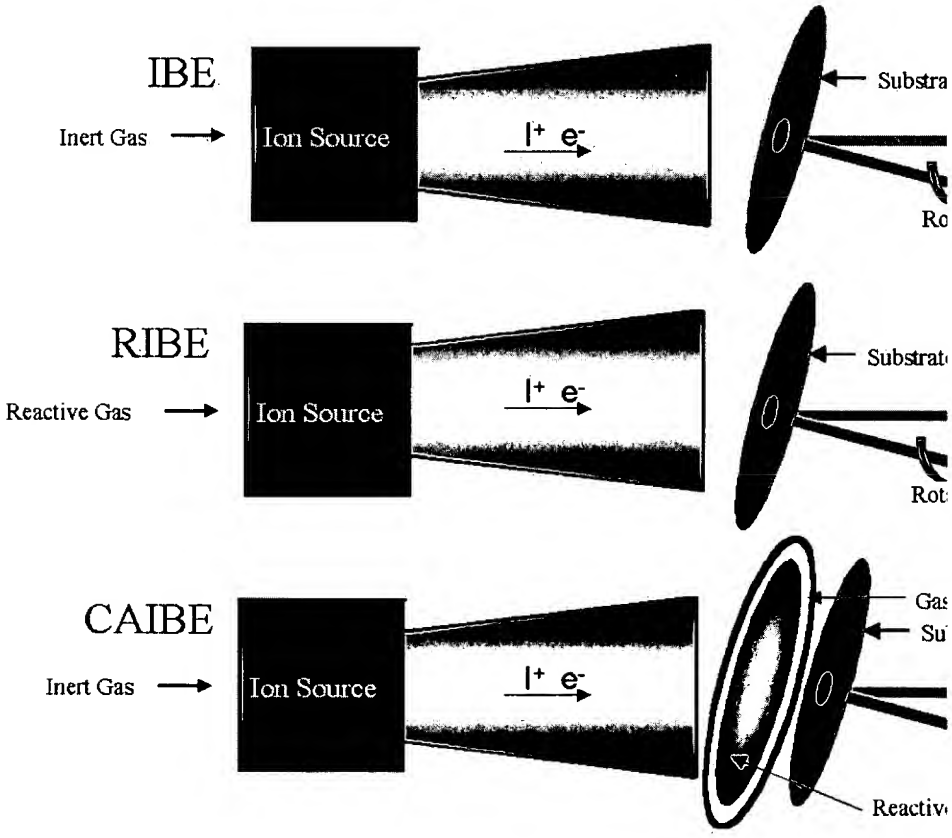
Ion Beam Etch

Ion beam etching (IBE) uses an energetic, broad beam collimated and highly directional i physically mill material from a substrate mounted on a rotating fixture with adjustable tilt a sources used are "gridded" ion sources of the Kaufman type and are typically neutralized independent electron source. Large and small ion sources are available (from Veeco Insti example) capable of uniform etching over areas as large as 9 inches in diameter. The hig directional ion flux allows for anisotropic etching of any material. The ability to modify the substrate allows the creation of processes that result in tailored sidewall profiles with mini redeposition on overlying masks.

Reactive ion beam etching (RIBE) is identical to IBE, except that reactive ions are incorpo or in part in the etching ion beam. In another variant known as chemically assisted ion be (CAIBE), reactive species are introduced into the process independent of the ion beam. F materials, systems RIBE and CAIBE offer additional control of etch anisotropy, sputter re etch rate over IBE.



Other technology:

Biased Target IBD | In-Situ Process Monitoring | Dynamic Process Compensat
Ion Beam Deposition | Direct IBD | Ion-Assisted Evaporation